Wishbone to FML caching bridge

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1 Specifications

This core gives access over a Wishbone link to a memory subsystem using the FML bus.

It can be used to connect the high-bandwidth parts of a system which use FML to a more traditional Wishbone system-on-chip base, which includes a CPU and low-speed peripherals.

To make efficient use of the burst-oriented FML bandwidth, the bridge implements a cache. This cache can cause coherency problems with other FML masters writing to the memory. To solve this issue, the bridge can be programmed to flush the cache.

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