AC'97 controller

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1 Introduction

The AC'97 controller core enables a system-on-chip (SoC) to interface directly with off-the-shelf AC'97 codecs popular in PCs.

It provides a cost-efficient solution to add good quality sound input and output to a FPGA-based system.

2 Registers

2.1 Codec register access, offsets 0x00, 0x04, 0x08 and 0x0c

Those registers are used to read and write the registers inside the off-chip AC'97 codec.

Register 0x04 holds the current register address, while registers 0x08 and 0x0c contain data respectively written to and read from the AC'97 codec.

Register 0x00 controls the transfers to and from the AC'97 codec registers. Its bits are mapped as follows:

Bit	Description
0	Request pending. Write 1 to this bit to initiate a read or write request.
1	Selects between a read (0) and write (1) request.
2–31	Reserved.

2.2 Downstream control registers, offsets 0x10, 0x14 and 0x18

Those registers control the stream of PCM data from the SoC to the AC'97 codec (audio playback).

The PCM data is transferred via DMA. Stereo samples are interleaved and use the signed 16-bit big-endian format. The sample rate is fixed at 48kHz.

The register 0x14 holds the current DMA address. It is incremented by 4 (two 2-byte values — one for each channel) after each transferred sample. The register 0x18 (counter register) holds the number of bytes that can still be transferred in the DMA buffer before a new buffer address must be programmed. It is decremented by 4 after each transferred sample. The maximum value is `0x3fffc`. When this register reaches 0, a "DMA read" interrupt is generated and the AC'97 controller uses its built-in FIFO to supply the codec with data.

The DMA address must be aligned on a 32-bit boundary, and the number of bytes must be a multiple of 4.

The register 0x10 controls the stream of data:

Bit	Description
0	Downstream enabled. When this bit is set by the CPU, the AC'97 controller sends PCM data to the codec and reads the DMA buffer (if the counter register is not zero).
1–31	Reserved.

2.3 Upstream control registers, offsets 0x20, 0x24 and 0x28

Those registers control the stream of PCM data from the AC'97 codec to the SoC (audio recording).

They work exactly like the downstream control registers.

3 Interrupts

The AC'97 core is equipped with 4 active-high edge-sensitive interrupt lines:

Line	Description
crrequest_irq	The codec configuration register read/write request has been sent.
crreply_irq	The value of a codec configuration register has been received (after a read request).
dmar_irq	The read (downstream/playback) DMA counter register has reached 0.
dmaw_irq	The write (upstream/recording) DMA counter register has reached 0.

4 Using the DMA engine

The downstream and upstream DMA engines work exactly the same, and can be enabled at the same time.

4.1 Initiating the stream

- Prepare a memory buffer. If you want to play sound, it must be initialized with the samples. If you want to record, it does not need to be initialized.

- Program the buffer address and the buffer length.

- Set bit 0 in the stream control register.

4.2 Refilling the stream

Once your buffer has been transferred, the AC'97 will send an interrupt to request another buffer.

- Prepare a new buffer.

- Program the new buffer address <u>then</u> the buffer length[1].

- Write any value to the stream control register to ack the interrupt (however, the bit 0 must still be set so that the stream continues).

4.3 Terminating the stream

Clear the bit 0 in the stream control register.

If the AC'97 controller is in the middle of a Wishbone bus cycle, this cycle will be allowed to finish. No new bus cycle will be started.

5 Connections

Port	Description
sys_clk	System clock.
sys_rst	System reset.
ac97_clk	AC'97 clock. Entirely asynchronous to the system clock.
ac97_rst_n	AC'97 reset signal (input).
ac97_sin	AC'97 serial data line (codec to SoC).
ac97_sout	AC'97 serial data line (SoC to codec).
ac97_sync	AC'97 synchronization line.
csr_*	CSR bus interface.
crrequest_irq	Codec register request sent interrupt.
crreply_irq	Codec register reply received interrupt.
dmar_irq	DMA read (downstream) interrupt.
dmaw_irq	DMA write (upstream) interrupt.
wbm_*	Wishbone master interface for DMA.

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[1]When the stream is enabled, the AC'97 controller starts making transfers on the bus as soon as the counter register is non-zero.