Minimac - the minimalist Ethernet MAC

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1 Overview

Minimac is a 10/100 Ethernet MAC for MII PHYs, built with minimal hardware resource usage in mind. It is designed for resource-constrained system-on-chips where basic network connectivity is desired.

It has the following features:

- CSR control interface efficiently connects the core to the Milkymist^{TM} architecture.
- WISHBONE master interfaces stream packets straight to and from system memory, minimizing on-chip data storage.
- Four hardware-controlled packet reception slots reduce the risk of lost data in case of high interrupt latency from the system CPU.
- Software generates and checks Ethernet CRCs and preambles.
- Full duplex (switched) operation only, without collision detection, retransmission nor MAC filtering.
- Bit-banged MDIO interface.

2 Setup register

Register	Bits	Description
0x00	0	RX reset. When this bit is active (default at reset), the reception FIFO is cleared and kept empty, the reception logic is set to expect a new packet, and no new transfers are made through the RX DMA interface. If the bit is set while in the middle of a WISHBONE bus cycle, that cycle is allowed to finish. Setting the RX reset bit does not modify the state of the RX slots.
–	1	TX reset. When this bit is active (default at reset), the transmission FIFO is cleared and kept empty, the transmission logic is set to expect a new packet, and no new transfers are made through the TX DMA interface. If the bit is set while in the middle of a WISHBONE bus cycle, that cycle is allowed to finish.
–	31 – 2	Reserved.

3 MDIO

The two MDIO pins (clock and bidirectional data) are controlled using a low-level, bit-banged interface on register 0x04.

Register	Bits	Description
0x04	0	Logic level driven to the MDIO data pin (if OE=1).
–	1	Logic level read from the MDIO data pin.
–	2	Output Enable (OE). When this bit is set, the SoC drives the bidirectional MDIO data pin.
–	3	Logic level driven to the MDIO clock pin.
–	31 – 4	Reserved.

4 Packet reception

There are four reception slots. When a packet arrives, the Minimac cores picks the loaded slot with the lowest number (first slot 0, then 1, etc.), DMA's the packet into the system memory at the address given by the slot, updates the slot's byte count according to the length of the packet, and updates the slot's state to "pending".

If a reception error occurs, of if the packet exceeds the Ethernet MTU, the whole packet is discarded and the slot's state is unchanged. However, some of the packet's data may have been transferred to the system memory; so software should consider that the contents of a DMA buffer attached to a loaded slot are undefined. DMA buffers should be made large enough to include a maximum length Ethernet packet with preamble and CRC. Raw packets are received entirely, including preamble, trailer and CRC.

Memory addresses must be aligned to a 32-bit boundary.

Register	Description
0x08	State of the slot 0 (see below).
0x0C	DMA address of the slot 0. This address is read-only for Minimac and may be re-used for another transfer without the need to reprogram it.
0x10	Reception byte count of the slot 0.
0x14	State of the slot 1.
0x18	DMA address of the slot 1.
0x1C	Reception byte count of the slot 1.
0x20	State of the slot 2.
0x24	DMA address of the slot 2.
0x28	Reception byte count of the slot 2.
0x2C	State of the slot 3.
0x30	DMA address of the slot 3.
0x34	Reception byte count of the slot 3.

State	Description
0 (empty)	Slot is empty. No valid DMA address has been specified for this slot. Software may program a DMA address and, then, set the slot state to 1. This state is the default at reset.
1 (loaded)	Slot is loaded with a valid DMA address, and is awaiting a complete packet reception to switch to state 2. Software may cancel the potential transfer by setting the state to 0. In this case, no new DMA transfers will be made for this slot, but if the core was in a middle of a WISHBONE cycle, that cycle will be allowed to complete.
2 (pending)	Slot has received a valid packet which has been fully transferred to the DMA buffer. The byte counter has been updated with the length of the packet. No further packet transfers will occur for this slot. The software can set the state to 0 to disable this slot, or to 1 to reload it for a new transmission.
*	All other state values are invalid and should not be used.

If one or more slots is in state 2, the RX interrupt line is set and kept asserted.

5 Packet emission

Minimac supports only one outstanding packet emission request.

When software writes a non-zero value the the remaining byte count register after having programmed the address of the DMA buffer, a packet is streamed from system memory and sent to the PHY. A full raw Ethernet packet must have been loaded in the memory, including preamble, trailer and CRC. The packet must be contiguous in memory, i.e. there is no support for scatter-gather techniques. The remaining byte count register will then decrement while the packet is being transferred. Once it reaches 0, transmission terminates and the TX interrupt line is pulsed. At the same time, the address register is incremented until it reaches the end of the packet. This implies that the software typically needs to re-load the address register to send a new packet.

Software can cancel the transmission of a packet by writing 0 to the remaining byte count register. No new WISHBONE DMA transfer will be started, but if the core was in a middle of a WISHBONE cycle, that cycle will be allowed to complete. Cancelling the transmission of a packet is discouraged as it is likely to cause an incomplete Ethernet frame to be sent over the network.

The DMA buffer must be aligned to a 32-bit boundary.

Register	Description
0x38	TX DMA address.
0x3C	Remaining TX byte count.

6 Memory system considerations

In order to reduce costs, Minimac does not provide enough on-chip storage to hold complete Ethernet frames and instead streams them to and from the system memory while they are being transferred over the medium. However, to cope with the latency stemming from this technique, Minimac provides a limited form of data storage consisting of the TX and RX FIFO buffers, each being able to store a few dozen bytes (the exact amount is configurable at synthesis time).

This scheme obviously assumes that the system memory infrastructure can provide enough bandwidth and low levels of latency to the Minimac DMA interfaces. In case it fails to do so, FIFOs can overflow or underflow. This can happen transitionally, for example if the memory system is temporarily overloaded by transfers made by other cores in the system on chip.

- if the RX FIFO overflows, reception is interrupted, the slot does not go into state 2 (the whole packet is dropped), the "RX reset" bit is set in the setup register (clearing the FIFO), and the RX interrupt line is asserted (and kept asserted until the "RX reset" bit is cleared). To recover from this state, software must clear the "RX reset" bit.
- if the TX FIFO underflows, invalid data will be sent on the Ethernet medium. The software is not notified and does not need to do anything to recover from this state, except retransmit the corrupted frame (higher level network protocols will typically do that).

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